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10/694,761	10/29/2003	Richard C. Foss	PAT 819-2	5285

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,761	FOSS, RICHARD C.	
	Examiner	Art Unit	
	Guy J. Lamarre	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/29/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- Pursuant to 35 USC 131, **Claims 1-55** are presented for examination.

Claim Rejections - 35 USC ' 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1.1 **Claims 1-55** are rejected under 35 U.S.C. 102 (b) as being anticipated by **Mazumder** '*An On-chip ECC Circuit for Correcting Soft Errors in DRAM'S with Trench Capicitors,*" IEEE Journal of Solid-state Circuits, Vol. 27, No. 11, Nov. 1992, pages 1623-1633- IDS of *10/29/03*).

As per Claims 1-55, Mazumder discloses equivalent ECC for data transfer/communication in VLSI memory wherein said ECC comprises global/local accesses to memory cell arrays/subarrays of plural rows/columns of cells/flip-flops/latches/memory-elements with appropriate circuitry for detecting/flagging/correcting of plural bit error, said plural rows/columns made up of data/parity bits, e.g., Fig. 1.

Mazumder discloses equivalent placement of VLSI memory in testing mode via powering up, initializing such VLSI memory and subsequent correcting errors in such VLSI memory on 2nd para., at page 1623.

Memory cell arrays are partitioned into plural subarrays of data/parity bis, e.g., col. 1 of page 1626 last para.

Error detection is effected via XOR/modulo/compare components, e.g., Figs. 2-4.

Error correction/purging is effected via bit inversion/complementing, e.g., page 1626 penultimate para.

Data reading/write/sensing/refreshing is effected via sensing components, e.g., sense amplifying circuitry at Figs. 2-3, page 1628 last para.

Local/global I/O access/sync control is effected via at, e.g., Table I, Figs. 4, 6-8 and page 1624 first para.

Local/global parity generation is effected via at e.g., Fig. 1 -horizontal/row, vertical/column, overall/global-.

Mazumder discloses equivalent RAM with ECC means for memory data access/reading/writing as seen, e.g., in Figs. 1-4.

As per Claim 1, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system for a memory comprising: a memory block for storing a data word and a corresponding row parity bit; and a row parity circuit for receiving the data word and the corresponding row parity bit from the memory block in response to a memory block access operation, the row parity circuit comparing parity of the data word against the corresponding row parity bit for generating an active local parity fail flag in response to parity failure.

As per Claim 2, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 1, further including a local data I/O circuit for coupling the data word between the memory block and global datalines, and for coupling the corresponding row parity bit between the memory block and the row parity circuit.

As per Claim 3, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 2, wherein the row parity circuit includes a serial parity chain for receiving the data word from the local data I/O circuit and for providing a parity output corresponding to parity of the local data, and a sense circuit for receiving the parity output and the corresponding row parity bit, for providing the active local parity fail flag if the

logic state of the parity output and the logic state of the local row parity bit mismatch.

As per Claim 4, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 3, wherein the serial parity chain includes an even parity line driven to a first logic level at one end thereof, and an odd parity line driven to a second logic level at one end thereof, the parity output being provided from the other end of the even parity line, and each parity circuit includes cross-over transistors for coupling the parity output to one of the first and second logic levels.

As per Claim 5, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 4, wherein the sense circuit includes a cross-coupled latch for receiving and latching the parity output, and a comparator circuit for comparing the latched parity output to the local row parity bit.

As per Claim 6, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 5, wherein the sense circuit includes switching means for coupling the latched parity output to the memory block during a write operation.

As per Claim 7, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 3, wherein the serial parity chain is segmented into at least two serially connected sub-parity circuits.

As per Claim 8, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 1, wherein the memory block includes one of redundant rows and columns, and corresponding redundancy circuits.

As per Claim 9, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 2, further including a parity block for storing a column parity word, each bit of the column parity word representing column parity for a corresponding bit position of the data word, a column parity circuit coupled to the local data I/O

circuit and the parity block for receiving the data word and the column parity word and for comparing column parity of each bit position of the data word to a corresponding bit of the column parity word in response to the active local parity fail flag, the column parity circuit inverting data of each bit position of the data word that fails column parity. **As per Claim** 10, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 9, wherein the memory block, the row parity circuit, the parity block and the column parity circuit are integrated in an embedded DRAM. **As per Claim** 11, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 9, wherein the parity block has a configuration identical to that of the memory block, and a parity block data I/O circuit for coupling the word of column parity bits between the parity block and the column parity circuit. **As per Claim** 12, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 10, wherein the column parity circuit includes a multiplexor circuit coupled between the local data I/O circuit and the global datalines for receiving the bits of the data word and for iteratively providing each bit of the data word to the global datalines, a parity block multiplexor circuit coupled to the parity block data I/O circuit for receiving the bits of the column parity word and for providing one bit of the column parity word in each iteration, a parity evaluator circuit coupled to the global datalines for receiving the one bit of the column parity word, the parity evaluator circuit comparing parity of the global datalines to the one column parity bit in each iteration and generating an active global parity fail flag in response to column parity failure, and a global dataline inverting circuit for receiving and then inverting data of the global datalines in response to the active global parity fail flag. **As per Claim** 13, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 12, wherein the multiplexor circuit and the

parity block multiplexor circuit each include a counter for controlling operation thereof.

As per Claim 14, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 12, wherein the parity evaluator circuit includes a serial parity chain coupled to the global datalines for providing a parity output corresponding to parity of the global datalines, and a sense circuit for receiving the parity output and the one bit of the column parity word, for providing the active local parity fail flag if the logic state of the parity output and the logic state of the one bit of the column parity word mismatch.

As per Claim 15, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 12, wherein the global dataline inverting circuit includes a flip-flop having an input coupled to one global dataline, an output coupled to a complementary global dataline of the one global dataline, a complementary output coupled to the global dataline, and a clock input for receiving the active global parity fail flag.

As per Claim 16, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 2, further including a column parity check circuit for selectively inverting bits of the column parity word on the global datalines in a write operation for writing a new word to an address of the data word stored in the memory block, the column parity check circuit including, a parity comparison circuit for storing the data word and the new word and for comparing each bit position of the stored data word to each corresponding bit position of the stored new word, the parity comparison circuit providing a mismatch flag signal for each bit position having mismatching logic states, and a parity inverting circuit coupled to the global datalines and for receiving the mismatch flag signals, the parity inverting circuit inverting the logic state of the global datalines in response to the corresponding received mismatch flag signals.

As per Claim 17, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 1, wherein the memory is a DRAM and the memory block access operation includes a refresh operation.

As per Claim 18, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 1, wherein the memory is one of an SRAM and an FeRAM, and the memory block access operation includes a data purge operation.

As per Claim 19, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of detecting and purging bit errors in a memory, comprising: a) executing a read operation to read a data word and corresponding row parity bit from a memory block of the memory; b) comparing row parity of the data word against the corresponding row parity bit and generating a row parity fail flag in response to row parity failure; c) comparing column parity of each bit of the data word against a corresponding bit of a column parity word stored in a parity block of the memory, in response to the row parity fail flag; and, d) inverting bits of the data word that fail column parity.

As per Claim 20, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 19, wherein the step of executing includes suppressing the data word from global I/O circuits.

As per Claim 21, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 19, wherein the step of executing includes providing the data word and the corresponding row parity bit to a local databus.

As per Claim 22, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 21, wherein the step of comparing row parity includes executing a row parity check of the local databus against the corresponding row parity bit.

As per Claim 23, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-

1633, equivalent method of claim 21, wherein the step of comparing column parity includes iteratively multiplexing bits of the data word from the local databus to a corresponding global dataline in response to row failure.

As per Claim 24, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 23, wherein the step of comparing column parity includes executing a column parity check of the global datalines against a corresponding column parity bit in each iteration.

As per Claim 25, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 24, wherein the step of comparing column parity includes inverting the data bits of the global datalines if column parity failure is detected in each iteration.

As per Claim 26, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 19, wherein the background read operation includes a refresh operation.

As per Claim 27, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 19, wherein the background read operation includes a data purge operation.

As per Claim 28, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 25, wherein the step of inverting includes inverting the data bit of a local databus line coupled to one of the global data lines for purging the bit error of the data word stored in the memory block.

As per Claim 29, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 23, wherein the step of iteratively multiplexing includes selectively activating column access transistors for coupling a different local databus line to the corresponding global dataline in each iteration.

As per Claim 30, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 29, wherein the step of selectively activating includes incrementing a counter to address and activate a different column access transistor in each iteration.

As per Claim 31, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 30, further including maintaining activation of the column access transistor corresponding to the memory block having row parity failure.

As per Claim 32, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system for a memory comprising: a plurality of memory blocks for storing data words and corresponding row parity bits, one of the memory blocks being a parity block for providing a column parity word; a local data I/O circuit coupled to each memory block for transferring the data words to global datalines; a row parity circuit coupled to the local data I/O circuit of each memory block for receiving the data words and the corresponding row parity bits in a memory block access operation, and for comparing parity of the data words against the corresponding row parity bits for generating a corresponding active local parity fail flag in response to row parity failure; and, a column parity circuit coupled to all the local data I/O circuits, the global datalines, and the parity block for receiving the data words and the column parity word, the column parity circuit iteratively transferring a bit from each of the data words to a different global dataline for comparing parity of the global datalines to a corresponding bit of the column parity word, the column parity circuit inverting data of the global datalines in response to column parity failure in each iteration.

As per Claim 33, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system of claim 32, wherein each row parity circuit includes a serial parity chain for receiving the data word from the local data I/O circuit

and for providing a parity output corresponding to parity of the data word, and a sense circuit for receiving the parity output and the corresponding row parity bit, for providing the active local parity fail flag if the parity output and the corresponding row parity bit mismatch.
As per Claim 34, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system of claim 33, wherein the serial parity chain includes an even parity line driven to a first logic level at one end thereof, and an odd parity line driven to a second logic level at one end thereof, the parity output being provided from the other end of the even parity line, and each parity circuit includes cross-over transistors for coupling the parity output to one of the first and second logic levels.
As per Claim 35, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system of claim 34, wherein the sense circuit includes a cross-coupled latch for receiving and latching the parity output, and a comparator circuit for comparing the latched parity output to the local row parity bit.
As per Claim 36, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system of claim 35, wherein the comparator circuit includes an exclusive OR gate.
As per Claim 37, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system of claim 32, wherein each memory block includes one of redundant rows and columns, and corresponding redundancy circuits.
As per Claim 38, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system of claim 32, wherein the parity block has a configuration identical to that of each memory block, and a parity block data I/O circuit for coupling bits of the column parity word to the column parity circuit.
As per Claim 39, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-

1633, equivalent error detection and purging system of claim 38, wherein the column parity circuit includes a multiplexor circuit coupled between each local data I/O circuit and the global datalines for receiving the bits of the data word and for iteratively providing each bit of the data word to the global datalines, a parity block multiplexor circuit coupled to the parity block data I/O circuit for receiving the bits of the column parity word and for providing one bit of the column parity word in each iteration, a parity evaluator circuit coupled to the global datalines and for receiving the one bit of the column parity word, the parity evaluator circuit comparing parity of the global datalines to the one column parity bit in each iteration and generating an active global parity fail flag in response to column parity failure, and a global dataline inverting circuit for receiving and inverting data of the global datalines in response to the active global parity fail flag.

As per Claim 40, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection system of claim 39, wherein the multiplexor circuit and the parity block multiplexor circuit each include a counter for controlling operation thereof.

As per Claim 41, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system of claim 39, wherein the global dataline inverting circuit includes a flip-flop having an input coupled to one global dataline, an output coupled to a complementary global dataline of the one global dataline, a complementary output coupled to the one global dataline, and a clock input for receiving the active global parity fail flag.

As per Claim 42, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent error detection and purging system of claim 32, further including a column parity check circuit for selectively changing bits of the column parity word on the global datalines in a write operation, for writing a new word to an address of the data word stored in the

memory block, the column parity check circuit including, a parity comparison circuit for storing the data word and the new word and comparing each bit position of the stored data word to each corresponding bit position of the stored new word, the parity comparison circuit providing a mismatch flag signal for each bit position having mismatching logic states, and a parity inverting circuit coupled to the global datalines and for receiving the mismatch flag signals, the parity inverting circuit inverting the logic state of the global datalines in response to the corresponding received mismatch flag signals.

As per Claim 43, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method for writing row and column parity bits to a memory system in a write operation, the memory system having a memory block for storing a data word and a corresponding row parity bit, and a parity block for storing column parity bits, the method comprising: a. latching a stored data word read out from an address to which a new data word is to be written; b. writing the new data word to the address and generating a corresponding row parity bit; c. comparing data between each bit position of the stored data word and the new word; and, d. inverting the column parity bits corresponding to mismatching bit positions.

As per Claim 44, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 43, wherein the step of latching includes reading the stored data word onto a global databus.

As per Claim 45, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 43, wherein the step of writing includes latching the new data word.

As per Claim 46, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 43, wherein the step of inverting includes reading the column parity bits onto a global databus.

As per Claim 47, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 46, wherein the step of inverting includes inverting the column parity bits of the global databus that correspond to bits of the stored data word that mis-match bits of the new data word.

As per Claim 48, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 43, further including a memory initialization step prior to the step of latching.

As per Claim 49, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 48, wherein the memory initialization step includes i. writing preset logic values to memory cells of an activated wordline, ii, reading out the preset logic values for latching by bitline sense amplifiers, and iii. activating all wordlines of the memory block to write the latched preset logic values thereto.

As per Claim 50, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 49, wherein the step of reading includes disabling bitline precharge and equalize circuits after the preset logic values are latched by the bitline sense amplifiers.

As per Claim 51, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 49, wherein the step of activating includes iteratively activating individual wordlines.

As per Claim 52, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 51, wherein the step of iteratively activating individual wordlines includes addressing each wordline with a refresh counter.

As per Claim 53, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 49, wherein the step of activating includes iteratively

activating multiple wordlines simultaneously.

As per Claim 54, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 49, wherein the step of activating includes simultaneously activating all wordlines.

As per Claim 55, Mazumder discloses, e.g., in Figs. 1-9 and related description on pages 1623-1633, equivalent method of claim 50, wherein the activated wordline includes a master wordline and the step of writing includes activating all column access devices to write the preset logic value to all the memory cells coupled to the master wordline.

Specification

2. The disclosure is objected to because the abstract exceeds 150 words. Appropriate correction is required.

Claim Objections

3. The claims recite, in passim, 'thereof' and/or 'thereto,' which is not clear. Appropriate correction is required.

Conclusion

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
7/17/2006